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PRODUCT SPECIFICATION

RB32KC

32K CMOS

BATTERY BACKED RAM BOARD

for NASCOM and GEMINI MICROCOMPUTERS

TECHNICAL SPECIFICATION OF MICROCODE 32K CMOS MEMORY BOARD

INDEX

Physical specification	page 1
Electrical specification	page 2
Functional description	page 3
Link selectors	page 5
Physical layout of link selectors	page 9
Examples of option link selections	page 10
Notes for Nascom users	page 12
Component lists	page 13
Circuit diagrams	page 14
Errata	page 15

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PHYSICAL SPECIFICATION

Board dimensions: 203.00mm wide by 203.00mm high

1.50mm resin bonded glass

1 ounce copper

Construction: double sided, through hole plated solder resisted
and silk screen printed.

Edge connector: 5 micron gold on copper

Board manufactured to BS9000 standard

ELECTRICAL SPECIFICATION

Maximum power consumption	250 mA at 5 volts
Standby current (back up mode)	120 microA maximum at 3.6 volts
Access time	165 nano seconds

(the above figures apply to fully populated 32K byte RAM board)

Maximum BUS signal load	½ standard TTL load
Voltage supply requirements	5 volts +/- 5%
Battery charge	100 mA Hours
Charge rate	1 mA
Charge:Discharge Ratio	10:1 minimum

FUNCTIONAL DESCRIPTION

IC17 and IC18 provide buffering of the address lines A0 to A10 and these signals are connected to IC1 - IC16 to provide the 2K address space occupied by each memory IC.

A11 is split into A11 and $\overline{A11}$ by inverter IC27b to provide a partially decoded chip select signal and determine which 2K byte IC is at the top or bottom of each 4K block.

A12 - A14 are decoded by the two three-to-one-of-eight decoders IC19 and IC20 to provide 16 4K byte block select signals. A15 is fed to the active-high enable on IC19 and to an active-low enable on IC20 thus decoding the block select outputs into two ranges 0 to 7 (covering address space 0000 hex to 7FFF hex) for the active low enabled IC20, and 8 to Fh (covering 8000 hex to FFFF hex) for the active-high enabled IC19. These active-low block enable signals are sent to the input of tri-state buffers IC30 - IC33. The outputs of the buffers being fed into the \overline{CS} pin of each memory IC.

The buffers are enabled by either signal A11 for the top half of the 4K block or signal $\overline{A11}$ for the bottom half of the 4K block. Thus the buffers for all \overline{CS} inputs on either the top half or the bottom half of each block are enabled simultaneously, however only one input to each buffer in either half will be low thus ensuring only one memory IC is enabled at a time.

The eight block enable signals selected from IC19 and IC20 are also provided as inputs to IC22, an eight input NAND gate. The output of the NAND will therefore be high when a 4K block is selected on this board. This active high signal is Nanded with the $\overline{RAM DIS}$ signal by IC34a and the output further ANDed with the decoded active-low output from IC23 to provide the active-low enable signal for the data-bus transceiver IC21.

The active-low output-enable and write-enable signals for each memory IC are commoned together into two separate sets comprising PAGE A (IC 1-8) and PAGE B (IC 9-16).

Each set of \overline{OE} and \overline{WE} is provided by the outputs of a pair of tri-state buffers (IC29). The active high enables of these tri-state buffers are commoned together and connected to the emitter of TR2.

IC28, TR1 and TR2 form a fast switching voltage level detector. This circuit has been set-up to switch TR2 on whenever the voltage V_{cc} drops below 4.5V, thus disabling all read and write signals. This ensures that no spurious data corruption results from the unpredictable behaviour of bus signals during a power down period. Further protection is provided by the gating of this signal with A11 and $\overline{A11}$ in IC26 c and d. Each of the inputs to the tri-state buffer IC29 is provided by the output of four two-input NAND gates IC25a - IC25d whose inputs are the inverted \overline{RD} bus signal for read enables or the inverted \overline{WR} signal for write enables and the output from the four 'D' type latches in IC24. The two \overline{RD} enable signals are also ANDed together to determine the direction of the data bus transceiver. A low on the direction-input to the transceiver enables the buffers in the data bus to memory board direction.

The four 'D' type latches controlling read and write enables are addressed at OFFH in the I/O space. This I/O address is decoded by IC23, a thirteen input NAND gate. The inputs to this NAND gate comprise A0 - A7, an inverted \overline{IORQ} (inverted by IC27d) and an inverted \overline{WR} signal (inverted by IC27f). The output of the NAND is used to provide the common clock on the four 'D' type latches.

The inputs to the latches are link selectable on to any of the data bus signals. The outputs Q or \overline{Q} are link selectable as the inputs to the four two-input NAND gates. (Thus allowing the option between enabling or disabling a page on RESET). RESET is connected to the common clear signal on the latches.

The output from the thirteen input NAND gate is also used to enable the data bus transceiver. The 10K pull-up resistors on address lines A0 - A10 and \overline{CS} , \overline{WE} , \overline{OE} of each memory IC are provided to ensure that the parameters for the low-standby current of the CMOS memory chips are met.

LINK SELECTORS

Links are provided on the board to select several options.

The links are made by insulated wire stripped at each end to expose 3 to 4 mm of conductor. The exposed conductor is pushed gently into the appropriate socket pin.

The diameter of conductor used should be 0.6 mm (24 S.W.G.) preferably gold or tin plated.

The various link selectors are named as follows:

LKSA:	Address boundary selection
LKSB:	Page selection
LKSC:	Page reset option
LKSD:	Power option
LKSE:	NAS-IO option

Layout of the link selection socket pins is provided in the silk-screening on the boards and also in the following figures:

LKSA	figure 1
LKSB	figure 2
LKSC	figure 3

LINKABLE OPTIONS

1. LKSA ADDRESS BOUNDARY OPTION

The address lines A12 - A15 are decoded into 16 4K blocks and these 16 active-low block select signals are brought out onto socket pins at LKSA.

In order to select a block boundary within a page, link the appropriate block decode signal (0-F) to one of the eight block enable pins. Where the board has been configured as two separate 16K pages it is possible to connect the same block decode signal to two block enable pins (one in each page). It is up to the users software to ensure that no two pages with blocks on the same addresses are both simultaneously read-enabled.

NOTE: NASCOM 1 users must also strap the NASMEM signal to one of the block decode signals (usually block 0)

SEE: 'Notes for Nascom Users'

2 PAGE CONFIGURATION, LKSB & LKSC

LKSB configures the board as either one 32K byte page or two 16K pages and selects which pages are to be used (0-3).

The board is controlled through two sets of read and write enable gates. REA and WEA are for bank A and REB and WEB are for bank B.

The decoded port address at OFFhex is used to enable the page control latch, the inputs to the latch are linked to the buffered data bus. When the board is configured as one page, LKSC signals REA and REB are commoned together, as are signals WEA and WEB. The buffered data bus is accessible by the adjacent 8 socket pins. The page mode scheme uses the low nybble as the page read enables and the high nybble is the page write enables. Thus if the board is configured as two pages (pages 0 and 3) data bit 4 is linked to WEA, data bit 0 to REA, data bit 7 to WEB and data bit 3 to REB.

On reset the latch outputs are reset, thus disabling the page/s. It may be a requirement of some systems to have a particular page enabled on reset, this can be achieved by strapping the relevant WE/RE signals to the \bar{Q} outputs from the latch at LKSC.

Permanent hardwired write protection is conveniently established by connecting the WEA and WEB pins to the two socket pins adjacent to LKSC.

3. POWER REQUIREMENTS OPTION

LKSD 1 to LKSD 16 are used to determine which memory I.C.'s will be provided with power from the on board battery during power down periods.

The common pin in each LKSD group labelled 'C' is connected to the pin labelled 'B' on each memory I.C. requiring the battery backup facility and to the pin labelled 'A' for each I.C. not requiring the back-up facility.

Due to space restriction on the board only A, B and C are silk screened.

It is important that memory I.C.s not designed for extremely low standby currents are not connected to LKSD-B, otherwise the excessive current drain will drastically reduce the available memory retention period. NMOS RAMS and all EPROMS should always be connected to LKSD-A.

The CMOS RAMS that are provided have been selected for standby currents of under 50 micro Amps.

The current drawn from the battery by each chip may be established by removing the board from the BUS and disconnecting the relevant I.C.'s LKSD and inserting a micro-ammeter between LKSD-C and LKSD-B. Chips drawing more than 100 micro Amps are not recommended to be connected to the battery.

The battery is rated at a normal 100 mAH at the discharge rate of 10mA. The boards supplied draw less than 120 micro Amps total giving over 1,000 hours (41 days) of retention during power down.

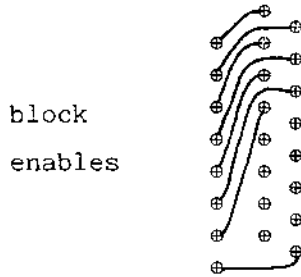
EXAMPLES OF OPTION LINK SELECTIONS

Example 1

One 32k Page

Addresses: 1000 hex - 8FFF hex

No paging



LKSA

block decodes



LKSB



LKSC

Example 2

Two 16k Pages

Page A

Addresses: 0000 hex - 0FFF hex, D000 hex - FFFF hex

Page numbers: 0 - 3 Hardware write protected

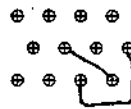
Page B

Addresses: 1000 hex - 4FFF hex

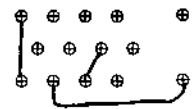
Page number: 0 Disabled on reset



LKSA



LKSB



LKSC

Note: Page A could contain a monitor and utilities.

Page B could be one of a number of work space areas.

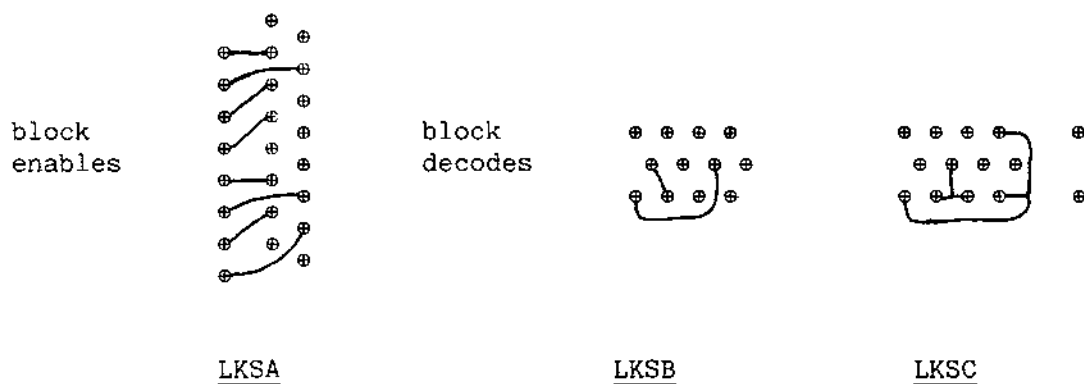
EXAMPLES OF OPTION LINK SELECTIONS

Example 3

One 32k Page

Addresses: 1000 hex - 4FFF hex, A000 hex - DFFF hex

Page number: 2 Enabled on reset



Example 4

Two 16k Pages

Page A

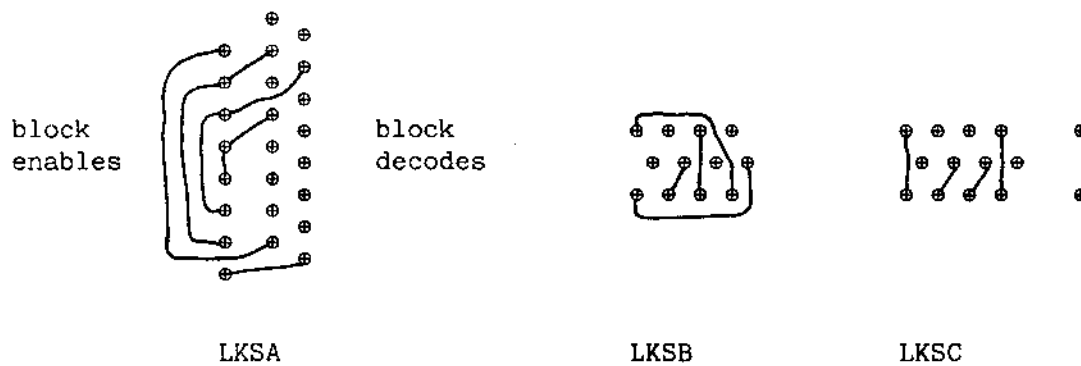
Addresses: 1000 hex - 3FFF hex, 8000 hex - 8FFF hex

Page number: 0 Enabled on reset

Page B

Addresses: 1000 hex - 3FFF hex, 9000 hex - 9FFF hex

Page number: 3 Disabled on reset



Note: Page 0 and page 3 must NEVER be read enabled at the same time
i.e. before enabling page 3 always disable page 0 and vice versa.

NOTES FOR NASCOM USERS

NASCOM I/O DECODE LKSE

NASCOM users who have not provided signal NAS-IO elsewhere in their system may do so at LKSE.

By strapping a link across LKSE, NASCOM 1 and 2 boards set to 'EXT I/O' will correctly decode the page control latch at 0FFh.

In fact LKSE is a link between address line A7 and NAS-IO so that the I/O address space has been split between 0-7Fh internal to NASCOM and 80-FFh external.

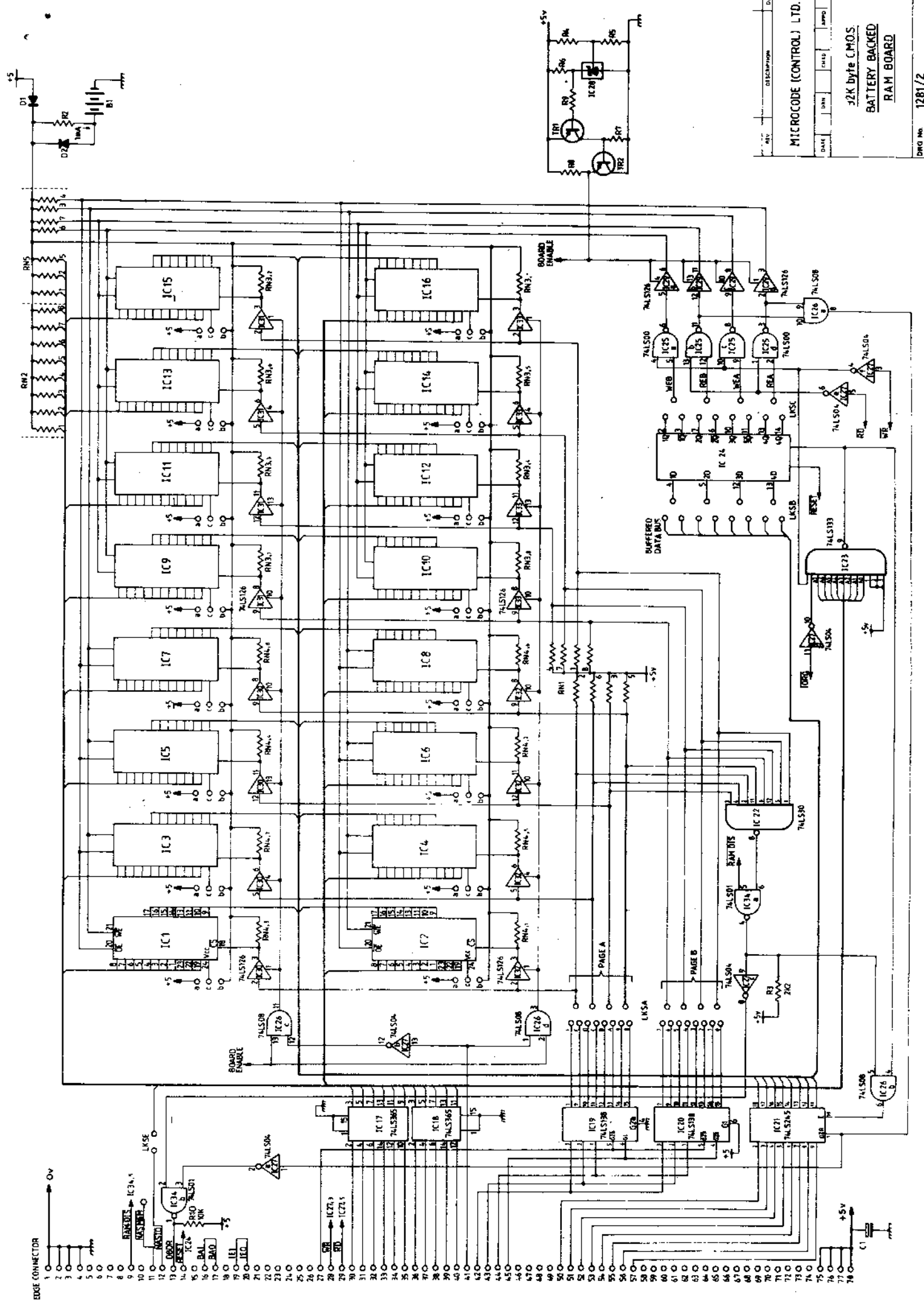
The block of eight port addresses on the NASCOM are still partially decoded but with the link LKSE strapped they will not repeat past 07Fh.

FOR NASCOM 1 USERS

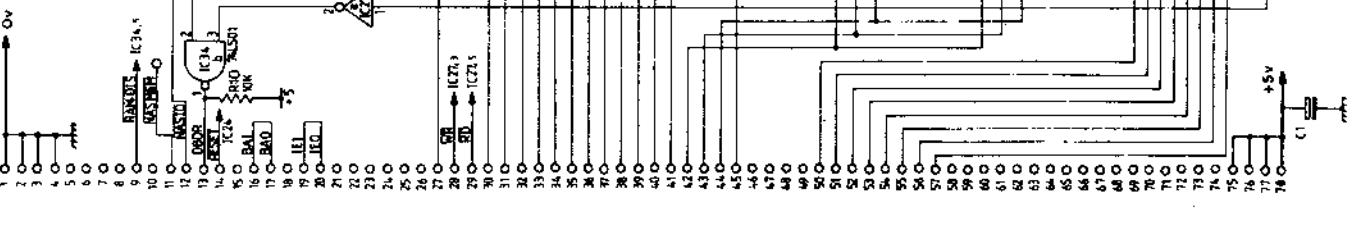
NASCOM 1 users using a buffer board for expansion must provide the signal NAS-MEM. NAS-MEM is an active-low signal which defines the 4K block of memory used internally by the NASCOM 1. Normally this will be decoded on block 0. The memory board provides a solder pad on the BUS line 11 (NAS-MEM) and this should have a wire link taken from it to the appropriate LKSA block decode signal. It is only necessary for one board in the system to provide this signal.

COMPONENT LIST

IC 1 - IC16	HM6116LP-3	2K byte-wide CMOS memory
IC17 - IC18	74LS365	Hex Tri-state buffers
IC19 - IC20	74LS138	Three to one of eight decoder
IC21	74LS245	Octal bi-directional buffer
IC22	74LS30	Eight input NAND gate
IC23	74LS133	Thirteen input NAND gate
IC24	74LS175	Quad D-type latch
IC25	74LS00	Quad two input NAND
IC26	74LS08	Quad two input AND gate
IC27	74LS04	Hex inverter
IC28	TL430C	Programmable zener
IC29 - IC33	74LS126	Quad buffer with active high enable
IC34	74LS01	Quad two input NAND gate open collector
TR1	BC559 or equivalent	PNP transistor
TR2	2N2906A or equivalent	PNP transistor
D1	0A202	Diode
D2	Not used	
C1	22 micro-F	Capacitor 10V W.D.C.
C3 - C18	10nF	Decoupling disc capacitors
RN1 - RN2	8 by 10K ohm	DIL resistor network
RN3 - RN5	8 by 2K ohm	DIL resistor network
R1	10K ohm	Resistor ¼ watt
R2	390 ohm	" " "
R3	2K2 ohm	" " "
R4	6K8 ohm	
R5	10K ohm	
R6	220 ohm	
R7	1K ohm	
R8	10K ohm	
R9	22K ohm	
R10	10K ohm	
B1	VARTEK MEMPAK 3.6v PCB Ni-cad Battery	
LKSA	24 off	
LKSB	12 off	
LKSC	14 off	Cambion Socket Pins
LKSD	48 off	450-0028-0103
LKSE	2 off	Gold plated socket pin



EDGE CONNECTOR



REV	DESCRIPTION	DATE

MICROCODE (CONTROL) LTD.

DATE	DESIGN	DRAWN	APP'D

32K Byte CMOS
BATTERY BACKED
RAM BOARD

DRG No. 1281/Z