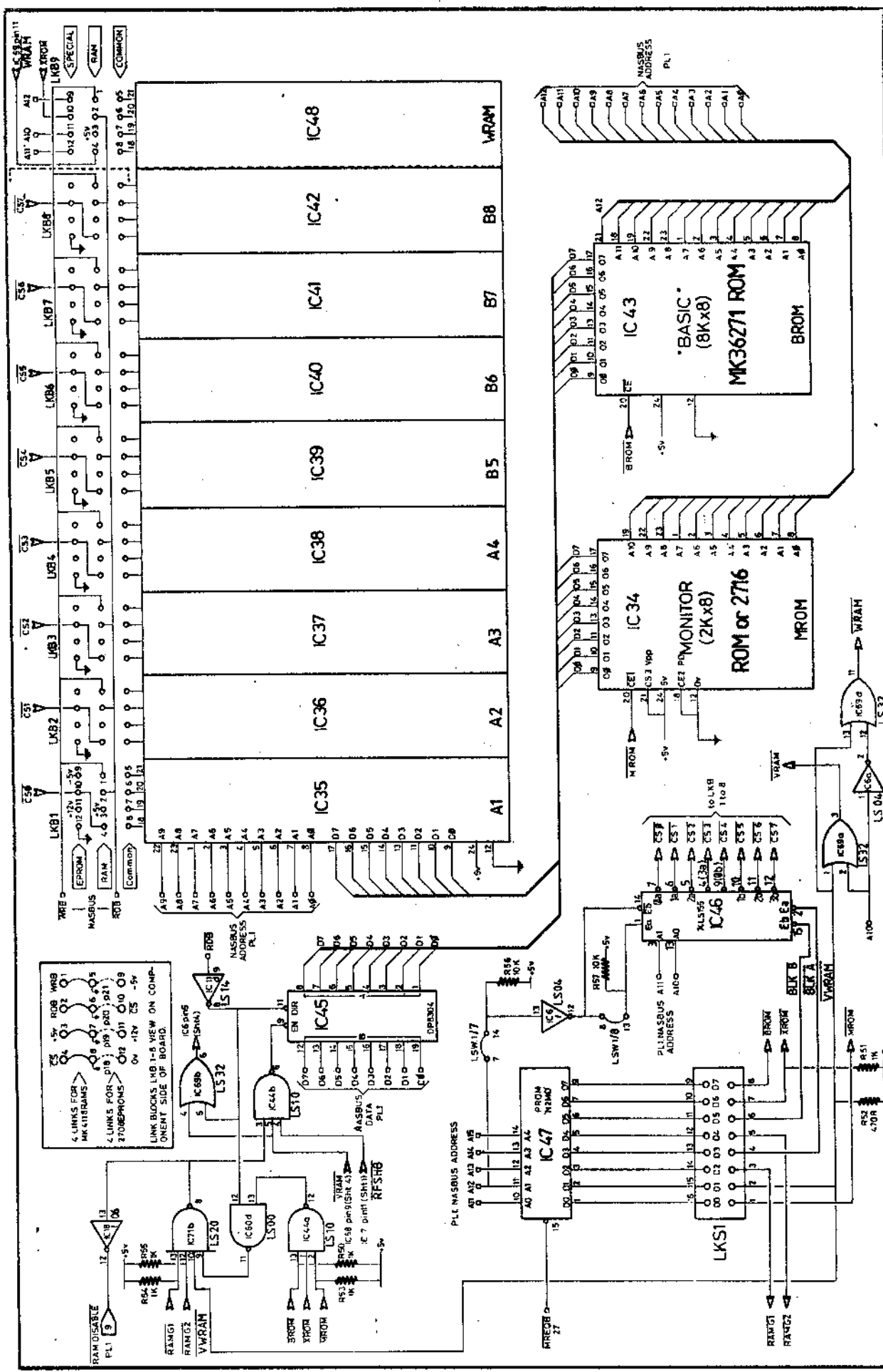


Issue 8 Sht 1 of 5 Drawn Checked Date 16-6-79
 Revisions:- revision 6/11/079 Drawing no. 022-401

NASCOM 2 CPU

Nascom Microcomputers

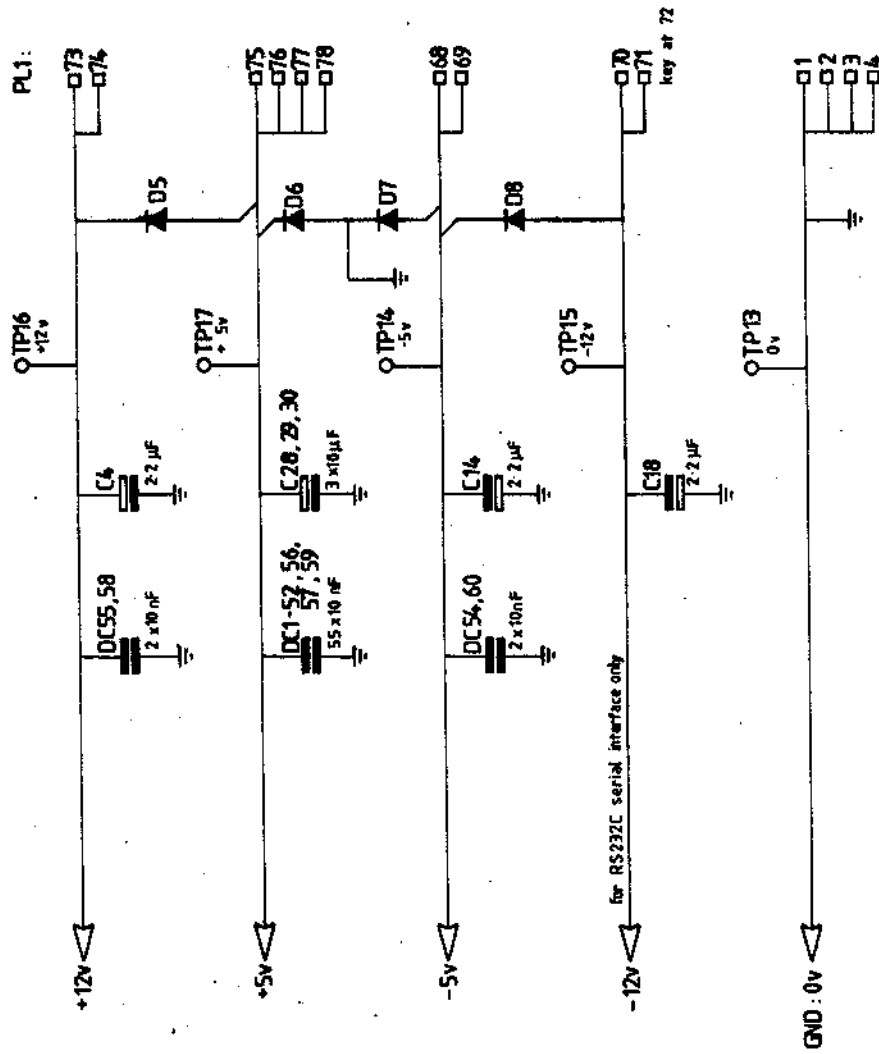
7-1 Circuit Diagrams



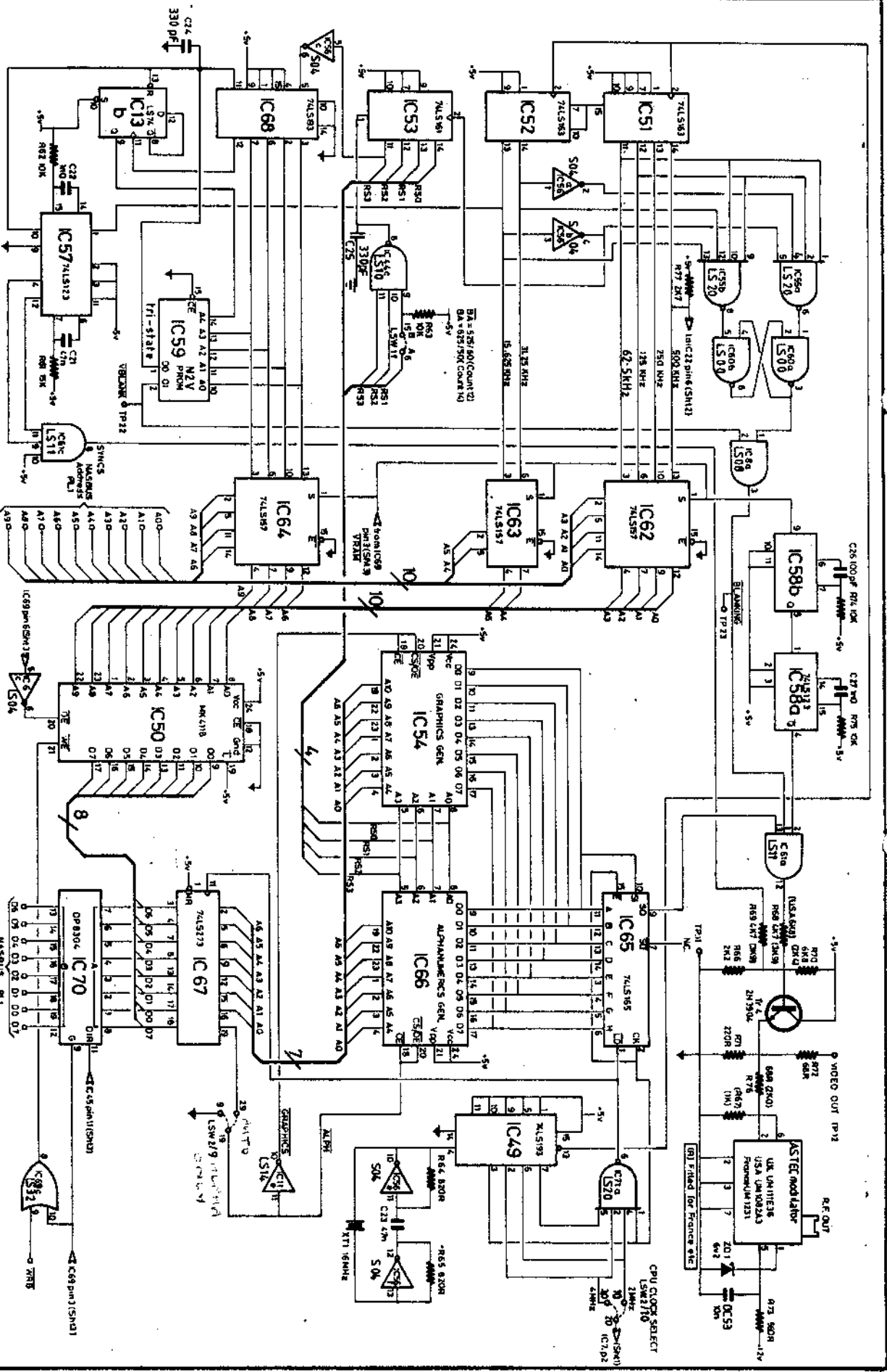
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NASCOM 2 Memory

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D5-7: 4 x 1N4001



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Issue 8 Sh14 of 5 Drawn Revisions

Checked

Date 20-6-79

Drawing no. 022-404

7.3 Relationship between N2MD PROM and link pins

It can be seen from circuit diagrams 3 and 4, that all on board memory (ICs 35;42, 48 and 50) is connected to address lines A0 to A9 which corresponds to 0000 - 03FFH or 1R of addresses. Additionally the MONITOR ROM is connected to A0 to A10 and the BASIC ROM to A0 to A12. The memory devices are enabled one at a time by means of a chip select or chip enable input, CS/CE (active low) which permits memory to be addressed at locations other than 0000H - 07FFH. The chip select function is performed by the N2MD PROM (IC47) in conjunction with the 16pin header plug (LKS1), IC6, IC46, IC69 and switches LSW1/7 and 8.

The MD PROM has 5 inputs (plus active low chip select) which are decoded by internal program, into 32 eight bit patterns, one for each combination of the input. The eight output lines are connected to one side of the 16 pin header. The outputs available from the N2MD PROM are as follows:-

		N2MD PROM					OUT-PUT BIT PATTERN								NORMAL USE	
		INPUT														
		A15	A14	A13	A12	A11	(XXXXX DECODE)	D7	D6	D5	D4	D3	D2	D1	D0	
0000H	-	0	0	0	0	0	(0 Low Half)	1	1	1	1	1	1	1	0	MROM (2K MONITOR ROM)
07FFH	-	0	0	0	0	0										
0800H	-	0	0	0	0	1		1	1	1	1	1	1	0	1	WRAM (2K WORKSPACE RAM)
0FFFH	-	0	0	0	0	1										
							(0 High Half)									
1000H	-	0	0	0	1	0	(1)	1	1	1	1	1	0	1	1	4K USER RAM (BLKA + RAMG1)
1FFFH	-	0	0	0	1	1		1	1	1	1	1	0	0	1	
2000H	-	0	0	1	0	0	(2)	1	1	1	1	0	1	1	1	4K USER RAM (BLKB + RAM G2)
2FFFH	-	0	0	1	0	1		1	1	1	1	0	1	1	1	
		0	0	1	1	0	(3)	1	1	1	1	1	1	1	1	
		0	0	1	1	1		1	1	1	1	1	1	1	1	
		0	1	0	0	0	(4)	1	1	1	1	1	1	1	1	
		0	1	0	0	1		1	1	1	1	1	1	1	1	
		0	1	0	1	0	(5)	1	1	1	1	1	1	1	1	
		0	1	0	1	1		1	1	1	1	1	1	1	1	
		0	1	1	0	0	(6)	1	1	1	1	1	1	1	1	
		0	1	1	0	1		1	1	1	1	1	1	1	1	
		0	1	1	1	0	(7)	1	1	1	1	1	1	1	1	
		0	1	1	1	1		1	1	1	1	1	1	1	1	
		1	0	0	0	0	(8)	1	1	1	1	1	1	1	1	
		1	0	0	0	1		1	1	1	1	1	1	1	1	
		1	0	0	1	0	(9)	1	1	1	1	1	1	1	1	
		1	0	0	1	1		1	1	1	1	1	1	1	1	
		1	0	1	0	0	(A)	1	1	1	1	1	1	1	1	
		1	0	1	0	1		1	1	1	1	1	1	1	1	
B000H	-	1	0	1	1	0	(B)	1	1	1	0	1	1	1	1	4K SPARE FOR EPROM
BFFFH	-	1	0	1	1	1		1	1	1	0	1	1	1	1	
C000H	-	1	1	0	0	0	(C)	1	1	0	1	1	1	1	1	4K SPARE FOR EPROM
CFFFH	-	1	1	0	0	1		1	1	0	1	1	1	1	1	
D000H	-	1	1	0	1	0	(D)	1	0	1	1	1	1	1	1	4K SPARE FOR EPROM
DFFFH	-	1	1	0	1	1		1	0	1	1	1	1	1	1	
E000H	-	1	1	1	0	0	(E)	0	1	1	1	1	1	1	1	MROM
		1	1	1	0	1	(F)	0	1	1	1	1	1	1	1	8K BASIC ROM
		1	1	1	1	0		0	1	1	1	1	1	1	1	
FFFFH	-	1	1	1	1	1		0	1	1	1	1	1	1	1	

PIN NAS ON LKS 1:

9 10 11 12 13 14 15 16

7.2 Contents of decode ROM's

I/O \$A0000.
 FF FF FF FF FF FF FF FF FD EF DF CF FF FF FF FF
 FE FB F7 EF FF CF FF CF FF FF FF CF FF FF CF FF
 #S1EE1. N2 I O/1
tristate or open collector

V \$A0000.
 FD FC FF FF FF FF FF FF FF FF FF FL FD FD FD FF
 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FD
 #S1FD1. N2V/2H
tristate

OP: \$A0000.
 01 00 03 03 03 03 03 03 03 03 01 01 01 01 03
 03 03 03 03 03 03 03 03 03 03 03 03 03 03 01
 #S0051. N2V/2L
tristate

MD \$A0000.
 FE FD FB FB F7 F7 FF FF FF FF FF FF FF FF FF
 FF FF FF FF FF EF EF DF DF EF EF 7F 7F 7F 7F
 #S1CE5. N2MD/3
open collector
(binary listing in text)

DB \$A0000.
 FC FC FE FE FD FE FD FC EC DD
 FC FC FE FE FD FE FD FC EC DD
 FC FC FE FE FD FE FD FC EC DD
 FC FC FE FE FD FE FD FC EC DD
 FC FC FE FE FD FE FD FC EC DD
 FC FC FE FE FD FE FD FC EC DD
 FC FC FE FE FD FE FD FC EC DD
 FC FC FE FE FD FE FD FC EC DD

N2DB/3H
tristate
(‘H’ version leaves
unused output bits
high)

\$A0000.
 EC EC EE EE EE EE 9E CE DD
 EC EC EE EE EE EE 9E 9E DD
 EC EC EE EE EE EE 9E CE DD
 EC EC EE EE EE EE 9E CE DD
 EC EC EE EE EE EE EC CE EE
 EC EC EE EE EE EE EC CE EE
 EC EC EE EE EE EE EC CE EE
 EC EC EE EE EE EE EC CE EE
 #S007C.

OP: \$A0000.
 7 4 7 4 7 6 7 5 7 6 5 7 4 6 5 5
 7 4 7 4 7 6 7 5 7 6 5 7 5 6 5 5
 7 4 7 4 7 6 7 5 7 6 5 7 4 6 5 5
 7 4 7 4 7 6 7 5 7 6 5 7 4 6 5 5
 7 4 7 4 7 6 7 5 7 6 4 7 4 6 5 5
 7 4 7 4 7 6 7 5 7 6 4 7 4 6 5 5
 7 4 7 4 7 6 7 5 7 6 4 7 4 6 5 5

N2DB/3L
tristate
(‘L’ version leaves
unused output bits
low)

\$A0000.
 6 4 6 4 6 6 6 6 6 6 1 6 4 6 4 4
 6 4 6 4 6 6 6 6 6 6 1 6 1 6 4 4
 6 4 6 4 6 6 6 6 6 6 1 6 4 6 4 4
 6 4 6 4 6 6 6 6 6 6 1 6 4 6 4 4
 6 4 6 4 6 6 6 6 6 6 4 6 4 6 6 6
 6 4 6 4 6 6 6 6 6 6 4 6 1 6 6 6
 6 4 6 4 6 6 6 6 6 6 4 6 4 6 6 6
 6 4 6 4 6 6 6 6 6 6 4 6 4 6 6 6
 #S057C.

7.4 Extracts from the Mostek Z80 central processing unit technical manual.

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